Simulation and Verification of Proposed Five Input Majority Logic Gates Using Quantum-dot Cellular Automata

Taylor Baldwin

Departmental Affiliation: Electrical and Computer Engineering
College of Engineering

Several proposed designs for five input majority logic gates have been introduced in quantum-dot cellular automata (QCA) literature and this project seeks to analyze these designs. QCA are an alternative to transistors because they take advantage of quantum effects to propagate a binary signal. The purpose of this research is to run simulations of two of these majority gates to verify their operational accuracy. A five input majority logic gate is especially useful within larger-scale QCA because it would help to minimize the overall number of cells needed for a specific QCA circuit. Our simulation runs a full-basis calculation for each possible fixed logic input (a 0 or 1) for all 32 cases present in each of the two circuits. This test is not redundant to the simulations within the literature because the proposed designs under test were simulated using approximations, like the intercellular hartree approximation. The results of our simulations verified the correct operation of one of these proposed five-input majority logic designs, however, because of symmetrical interference within the cells, one of the designs was in reality rendered inoperative. The findings of this research will be submitted to the *Journal of Microelectronics* in April of 2014.

Information about the Author:
Taylor Baldwin is a senior electrical engineering student who has worked on several research projects, presented several posters, and is a published author in the field of Quantum-dot Cellular Automata. He will be attending graduate school in the field of nuclear engineering specializing in fission studies in the fall of 2014.

Faculty Sponsor: Dr. Jeff Will, Dr. Doug Tougaw

Student Contact: aaron.baldwin@valpo.edu